WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a central processing unit;

an instruction cache in communication with the central processing unit;

a data cache in communication with the central processing unit;

a trace recorder operable to capture selective information passed from the central processing unit to the instruction cache and the data cache.

2. The integrated circuit of Claim 1, wherein the trace recorder is operable to capture information pursuant to a triggering event.

3. The integrated circuit of Claim 2, wherein the trace recorder is operable to maintain captured information prior to and associated with the triggering event.

4. The integrated circuit of Claim 2, wherein the trace recorder is operable to capture information subsequent to and associated with the triggering event.

5. the integrated circuit of Claim 2, wherein the trace recorder is operable to capture information associated with the triggering event prior to and subsequent to the triggering event.

6. The integrated circuit of Claim 1, wherein the trace recorder is operable to inhibit capturing of information.

7. The integrated circuit of Claim 1, wherein the trace recorder is operable to provide captured information to a device external to the integrated circuit.

8. The integrated circuit of Claim 1, wherein the trace recorder is operable to store captured data in non-consecutive storage locations.

9. The integrated circuit of Claim 1, wherein the trace recorder is operable to capture data every Nth operating cycle of the central processing unit.

10. The integrated circuit of Claim 1, wherein the trace recorder is operable to maintain captured information associated with a first trigger event despite the occurrence of a second trigger event.

11. A method of recording trace data in a microprocessor based integrated circuit, comprising:

identifying a triggering event;

capturing information transferred from a central processing unit to an associated instruction cache pertaining to the triggering event;

capturing information transferred from a central processing unit to a data cache pertaining to the triggering event.

12. The method of Claim 11, wherein information pertaining to a triggering event is captured prior to the triggering event.

13. The method of Claim 11, wherein information is captured in non-consecutive storage locations.

14. The method of Claim 11, further comprising:

outputting captured information.

15. The method of Claim 11, wherein information is captured for every Nth cycle associated with the operation of the central processing unit.

16. A trace recorder for a microprocessor based integrated circuit, comprising:

a memory array operable to capture information passed from a central processing unit to instruction and data caches of the integrated circuit;

a trigger control register operable to initiate information capture;

a capture control register operable to determine how information is to be captured and maintained;

an order map register operable to determine where information is to be captured within the memory array.

17. The trace recorder of Claim 16, further comprising:

an inhibit mask register operable to selectively inhibit capturing of information.

18. The trace recorder of Claim 16, further comprising:

controller logic operable to access the memory array according to the trigger control register, the capture control register, and the order map register.

19. The trace recorder of Claim 18, wherein the controller logic generates memory addresses to the memory array.

20. The trace recorder of Claim 16, wherein information is captured prior to and subsequent to a triggering event.